Call for Designs

University LSI Design Contest
ASP-DAC 2025

http://www.aspdac.com/
January 20-23, 2025
Tokyo, Japan

Aims of the Contest:

As a unique feature of ASP-DAC 2025, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Implemented on FPGAs/chips in universities or other educational organizations during the last two years.
(2) Designs that report actual measurements from implementations.
(3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.
Methods or technology used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2-4 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at **http://www.aspdac.com/**

Deadline for summary:	5 PM AOE (Anywhere on Earth)	August 2 (Fri), 2024
Notification of acceptance:		Sep. 16 (Mon), 2024
Deadline for camera-ready:	5 PM AOE (Anywhere on Earth)	Nov. 8 (Fri), 2024

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

(1) Novelty of application, algorithm, architecture, design, measurement, etc.
(2) Quality of design and implementation.
(3) Performance of the design.

Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2025. A separate poster session will be arranged to enable interactive discussion with the audience. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2025-udc@aspdac.com

ASP-DAC 2025 Chairs

General Chair:	**Yuichi Nakamura (NEC)**
Technical Program Chair:	**Yu Wang (Tsinghua University)**
Technical Program Vice Chair:	**Takashi Sato (Kyoto University)**
Design Contest Co-Chairs:	**Shinya Takamaeda-Yamazaki (The University of Tokyo, Japan)**
	Mahfuzul Islam (Kyoto University, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM